Limitation of initial surge in Latching Current Limiters (LCL)

Agnaldo Vieira Dias
Divisão de Eletrônica Espacial e Computação
Instituto Nacional de Pesquisas Espaciais - INPE
São José dos Campos - Brazil
agnaldo.dias@inpe.br

José Antenor Pomilio
Faculdade de Engenharia Elétrica e de Computação
Universidade Estadual de Campinas
Campinas - Brazil
antenor@fee.unicamp.br

Saulo Finco
Divisão de Concepção de Sistemas de Hardware
Centro de Tecnologia da Informação Renato Archer - CTI
Campinas - Brazil
saulo.finco@cti.gov.br

***Abstract*— DC power systems are widely used in the automotive and aerospace industries, with increasing requirements for voltage and current levels. Furthermore, there is a growing trend in utilizing DC power systems in microgrids. This increased adoption requires the development of more efficient protection mechanisms for reliable and secure operation.**

The latching current limiter (LCL) is essential in DC systems, designed to protect them against overload. It acts as a safeguard, preventing excessive current from damaging sensitive circuitry and components. Implementing an LCL provides critical protection for components, extending their lifespan and enhancing overall system reliability.

One issue concerning the LCL's operation is the initial surge. When an overload occurs, a peak current can flow through the circuit. This current could generate negative effects such as spikes in the DC power bus, interference and other undesirable consequences.

This work presents some methods to reduce or to eliminate the LCL switch's initial surge current. Traditional methods (reduction in VGS and use of output inductor) and new solutions (source inductor, impedance multiplier and predictive control) are explored. The results are compared and each method's advantages and disadvantages are show.

Keywords*— *DC power system, power line protection, current limit protection, latching current limiter (LCL), surge current

I. INTRODUCTION

In space missions, the distribution system is the circuitry responsible for connecting the DC power bus to the loads. It can provide fault protection and turn the loads on and off. The distribution system can use different methods to transfer power and protect the bus against failures in the loads [1]. Fuses are the simplest devices to isolate DC power buses from overload. However, the actuation of fuses can generate high spikes due to the inductive characteristic of the harness. Such spikes are potentially dangerous to the power bus and to the loads. Fuses also aren't able to provide current limitations during the fault [2].

To avoid these surges, a switching device called LCL (Latching Current Limiter) was introduced. These LCL switches turn power on and off, control the equipment inrush current and protect the DC power bus against faults, using the current limiting feature to avoid surge current. These functions increase the reliability of the electrical power systems [2].

The basic diagram of the LCL is shown in Fig. 1. When the LCL switch is turned on, the power MOSFET is in the ohmic region and, when a failure occurs, its operation shifts to the saturation region. In saturation, the current value will be limited by the control unit, that applies the proper V_{GS}.

Initially, the LCL switch remains deactivated while the bus voltage is applied to the "Input" terminal. When it receives a command at the "On/Off" terminal, a controlled soft turn-on of the MOSFET is initiated, leading to a gradual rise in current at the "Output" terminal (instant A in Fig. 2). The current sensor's readings are then transmitted to the control unit. Once the current reaches the designated nominal protection value (I_{NOM}), the control unit regulates the MOSFET gate voltage to maintain the current at a constant level (instant B in Fig.2). This constant current persists until the input capacitance of the load (instant C) becomes fully charged, resulting in a subsequent decline and stabilization of the current at the load's specified level (I_{LOAD}). To minimize conduction losses, the control unit places the MOSFET in the ohmic region, reducing the voltage drop across the LCL.

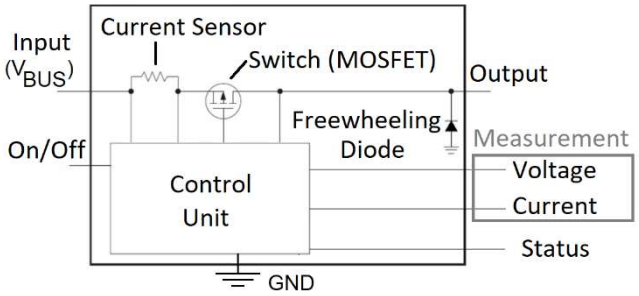

Fig. 1. Basic diagram of LCL switch [3]

In a malfunction situation (instant D), a rapid surge current occurs, surpassing the predefined threshold (instant E). The magnitude of this surge current is related to numerous factors including bus short-circuit impedance, harness impedance, load filter capacitance value, and more. The control unit's response dictates the duration of the surge event. It has to bias the MOSFET into the saturation region, decreasing the current back to its nominal value (instant F). At the instant E, the LCL initiates a countdown sequence. If the load reverts to its typical condition ($I_{LOAD} < I_{NOM}$), the current limitation forced by the LCL is finished, and the countdown timer is reset. However, if the timer expires (instant G), the control unit triggers the deactivation of the MOSFET, leading to a shutdown of the load. The freewheeling diode ensures a discharge path for the energy stored in the harness due to its inductive characteristics. The discharge process will continue until the instant H, when the current reaches zero.

This project is partially funded by the National Council for Scientific and Technological Development (CNPq) under grant #303859/2020-2.

At the beginning of the overload (Fig. 2 – from D to F), the control unit is not modulating the VGS effectively, so a surge current can flow through the circuit. This current will persist until the control unit of the LCL can act, changing the biasing of the MOSFET. These surge currents can reach high values, which can generate dangerous effects on the DC bus. Moreover, these surges have high rates of current variation (di/dt), which can generate electromagnetic interference. To avoid these problems, some techniques must be applied in the design of the LCL, to limit the peaks and high di/dt of surges.

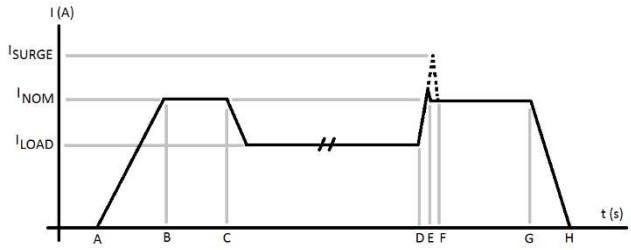

Fig. 2. Time diagram of an LCL switch [2]

II. METHODS TO REDUCE THE SURGE CURRENT

A. *Reducing the VGS of the power MOSFET*

The power MOSFET of the LCL switch operates normally in the ohmic region, and when a failure occurs, its operation is shifted to the saturation region. In saturation, the value of the current will be determined by VGS, as the influence of VDS in this situation is very low [4]. An example of ID (drain current) curves as a function of VDS, for various values of VGS, is shown in Fig. 3. In the figure, it's possible to see that VGS influences the transistor's behavior in the ohmic region, causing the device's conduction resistance to increase for lower applied VGS.

One way to reduce the peaks during the beginning of overload is by choosing a VGS value that can ensure low losses during the normal conduction of the LCL switch and, in the event of a short circuit, can keep the surge inside an appropriate range [5]. This technique helps in reducing the surge but cannot eliminate it.

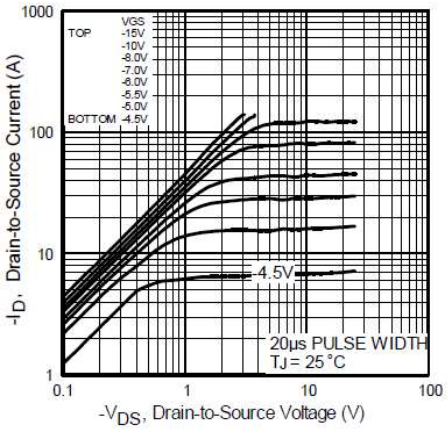

Fig. 3. Typical output characteristics of P-MOSFET [6]

Fig. 4 shows the result of the simulation for the initial surge current when a set of VGS values are applied to the power transistor (from -4.5V to -7.5V). As the VGS voltage value is increased (that means the module of VGS voltage is decreased), a reduction in the peak current value is observed. By selecting appropriate VGS values, a result is achieved where the switch losses are low, and the peak value is reduced. In Fig. 4, it is clear the surge has a short duration (near 5µs), but its peak value remains very high, more than ten times higher than the limiting value, 6A, proving the limited effect of this method.

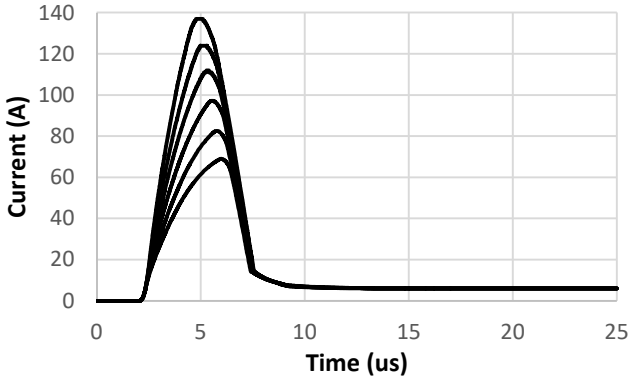

Fig. 4. Initial surge current for reduced VGS

B. *Insertion of an inductor in the output of LCL*

Another approach to reducing the intensity of current surges is the use of an inductor in series with the output of the LCL [5], as shown in Fig.5. With the insertion of the inductor, the circuit presents zero impedance for normal operation (DC current), but when a transient occurs, the inductor limits the current growth. This behavior of the inductor provides to the control unit the necessary time to act on the MOSFET and limit the surge during the transient. Additionally, the current variation (di/dt) in the circuit will be limited by the inductor. The initial di/dt can be estimated by

$$\frac{di}{dt} = \frac{V_{BUS}}{L_O} \quad (1)$$

where VBUS is the DC bus voltage applied to the "Input" terminal and LO is the inductance of the inserted inductor.

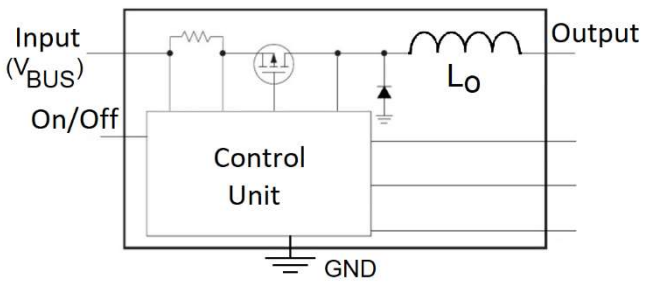

Fig. 5. Inductor in the output of LCL switch

Fig. 6 shows the result of the simulation for the initial surge current when different values of output inductors are used in the circuit (from 1µH to 30µH). As the value of the inductance is increased, a reduction in the peak current value is observed, and the lowest observed peak was 13.1A, measured when the value of the inductance was 30µH. The

minimum value of di/dt was 0.92A/µs and was measured for the same value of inductance. Even though the higher the inductance value, the lower the peak current value, the high inductance values will result in larger physical components, which can affect the size and mass of the final solution. Therefore, it is necessary to choose an inductance value that satisfies this trade-off relationship. The freewheeling diode inside the LCL will provide the path to discharge the energy stored in the output inductor and in the harness.

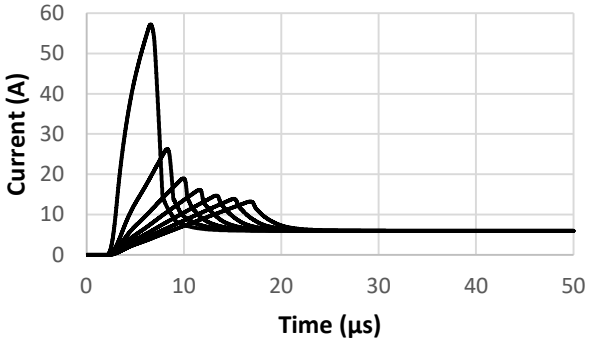

Fig. 6. Initial surge current using the output inductor

C. *Insertion of an inductor in the source of the power MOSFET*

The natural parasitic inductance in the source of the MOSFET is an element that limits the switching speed of the transistor, and the higher the value of this inductance, the slower the transitions are [7]. One way to limit the current variation through the circuit in case of load failure is to increase this inductance by inserting an inductor in the source terminal of the MOSFET [8], as shown in Fig. 7. A diode has to be inserted in parallel to discharge the inductor's energy during turn-off (freewheeling diode), preventing surges on the power transistor. Another way to represent this circuit in the moment of the short-circuit is shown in Fig. 8. The biasing of the MOSFET is provided by the source V_G; the source inductor is L_S; the V_{BUS} source represents the DC bus.

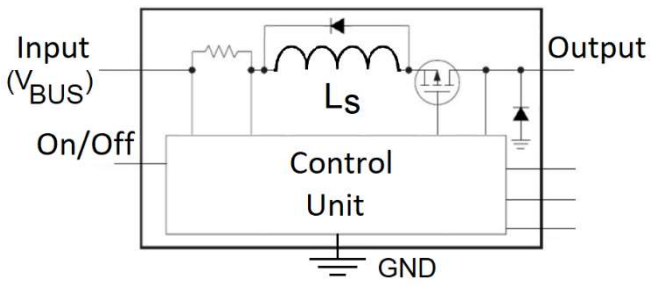

Fig. 7. Inductor in the source terminal

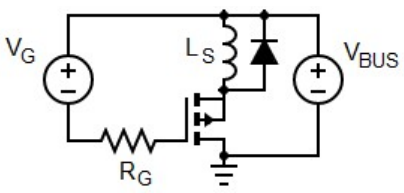

Fig. 8. Equivalent circuit using source inductor

In normal operation, the current through the circuit is stable, the voltage over L_S is almost zero, and the V_{GS} voltage is practically equal to the V_G voltage. When a failure occurs, there is a tendency for an abrupt change in the current. However, since the inductor L_S is in the current path, it opposes this current change, increasing a voltage drop over L_S (V_{LS}). As a result, the value of V_{GS} is no longer equal to the V_G voltage and becomes

$$V_{GS} = V_G - V_{LS} \cong V_T \quad (2)$$

where V_T is the threshold voltage of the power MOSFET.

As a result, the transistor has its bias voltage reduced and begins to operate in the saturation region. Fig. 9 shows the transient simulation for different values of inductor L_S. As the inductance value increases (from 0.5µH to 5µH), the current slope (di/dt) decreases, reaching 0.38A/µs. Additionally, as the inductor value increases, the current growth becomes almost linear for a longer period. In this region, the value of di/dt can be calculated by

$$\frac{di}{dt} = \frac{V_{LS}}{L_S} = \frac{V_G - V_T}{L_S} \quad (3)$$

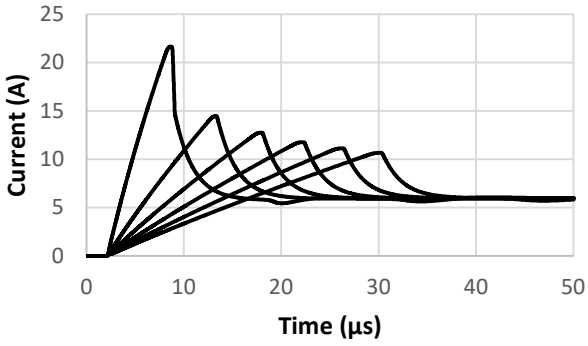

Fig. 9. Behavior of I_D related to increasing of L_S inductance

As shown in Fig. 9, as the value of the inductance in the source is increased, a reduction in the peak current value is observed. In the case of using the output inductor, the current growth is influenced by the bus voltage value. However, in the case of the use of the source inductor, the current growth is determined by the V_G voltage and the transistor threshold voltage (V_T), resulting in a lower inductance value for the same reduction in di/dt.

D. *Limiting the voltage over the source inductor*

One way to increase the effect of the inductor at the source terminal is by limiting the voltage drop over it [8]. The circuit that performs this function can be seen in Fig. 10. A diode (D_1), a transistor (Q_1), and a resistor (R_S) are added to the LCL design. During the transient, when the voltage over the inductor tends to be greater than the sum of the diode forward voltage (V_{D1}) and the transistor Q_1 emitter-base voltage, a current will flow through the resistor R_S, making Q_1 conduct and stabilize the voltage across the inductor. This circuit is an impedance multiplier that increases the effect of the source inductor. The value of di/dt can be calculated by

$$\frac{di}{dt} = \frac{V_{LS}}{L_S} = \frac{V_\gamma + V_{EB}}{L_S} \quad (4)$$

where Vγ is the threshold voltage of the diode D1 and VEB is the emitter-base voltage of the bipolar transistor Q1.

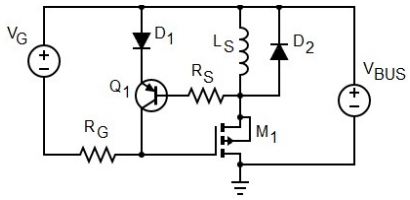

Fig. 10. Limiting the voltage over the source inductor

Fig. 11 shows the result of the simulation of the circuit using the impedance multiplier, where the value of the source inductance is increased, from 0.5µH to 3µH. In the case of using the source inductor, the current growth is determined by the VG voltage and threshold voltage and to achieve lower surge values, higher inductance or lower bias voltages (VG) are needed, implying higher losses. Using the impedance multiplier, the voltage applied to the gate terminal is controlled by the bipolar transistor during the transient, allowing the use of higher VG voltages and reducing the conduction losses of the MOSFET. The value of the source inductance is multiplied, demanding a smaller inductance to achieve the same di/dt.

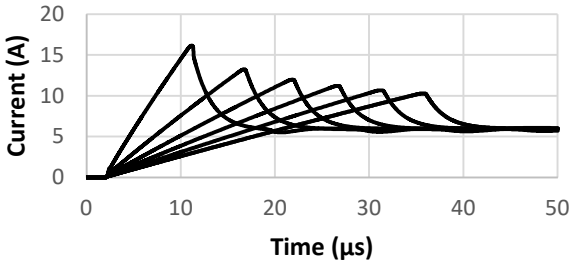

Fig. 11. Limiting di/dt using impedance multiplier

E. *Predictive control*

The use of reduced gate voltage, series inductor, source inductor and limiting voltage over the source inductor are some methods to decrease the initial current peaks [8]. Nevertheless, a surge current still can flow through the circuit when the overload situation begins.

The control loop of the LCL switch is shown in Fig. 12. When a low-impedance transient occurs in the load, there is a fast growth in the current, allowed by the limited response time of the control loop. To eliminate this delay (and reduce the surge current), a predictive control of current can be inserted in the LCL control unit [8], as shown in Fig. 13.

When a short circuit occurs in the load, there is an increase in the voltage across the inductor before the increase in the current through the circuit. If a sample of this inductor voltage (which is the derivative of the current) is inserted into the control loop, it can accelerate the controller response and soften the initial current surge. Fig. 13 illustrates this modification in the feedback diagram of the LCL, where the voltage drop over the inductor is injected into the control loop with the proper gain, provided by the Gd amplifier.

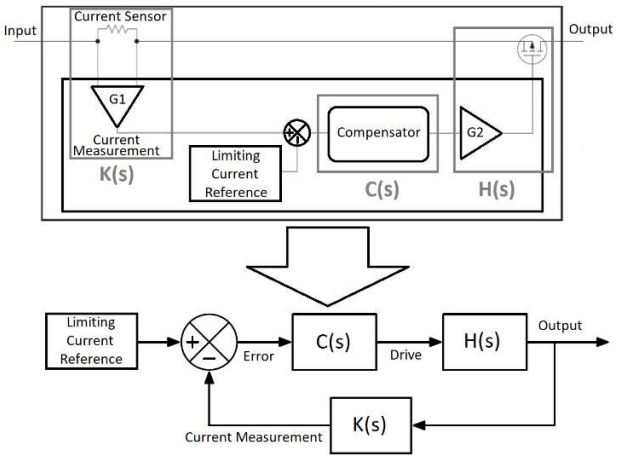

Fig. 12. Feedback loop of LCL switch [8]

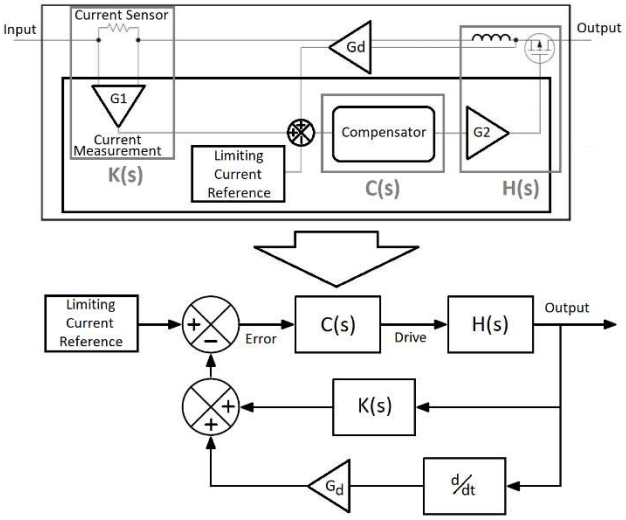

Fig. 13. Feedback loop using predictive controller [8]

Fig. 14 shows the result of the simulation for the initial surge current when different values of gain are used in the amplifier Gd. As the value of the gain is increased, a reduction in the peak current value is observed, changing to an overdamped waveform and eliminating the surge. This method can be used only in circuits that have an inductor in the current path.

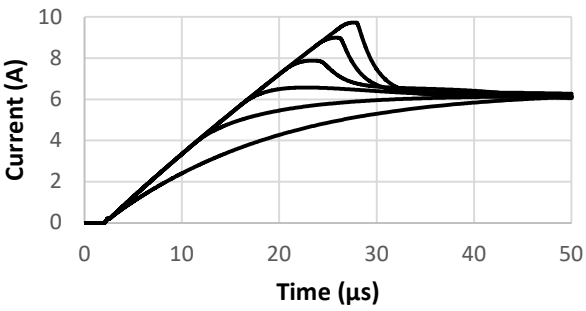

Fig. 14. Effect of predictive controller

III. Experimental Results

An LCL switch was designed to protect a 28V DC bus, with a current limitation set at 6A, a trip-off time of 2ms, a gate voltage of 6.2V, and di/dt of 1A/µs. The power MOSFET used is IRF5M4905 and the goal was to eliminate the initial surge.

In the first circuit, only the reduced gate voltage was applied (4.5V). Fig. 15 shows the current transient waveform in a short-circuit test. It can be observed that the current is limited to 6A after 9µs. However, before the current limitation, a current surge of nearly 70A with a di/dt of 50A/µs flows through the circuit. The result was very poor, with no di/dt control and a high surge current. Lower V_{GS} voltages were not used as it would result in high conduction losses.

In the attempt to reduce the initial surge, an inductor in series with the switch was used. The inductance value was defined based on the desired current variation (di/dt) and the DC bus voltage. Applying (1) and considering di/dt of 1A/µs and the nominal voltage of 28V, the inductance value should be 28µH. For convenience, a value of 30 µH was used and a gate voltage of 6.2V was applied to the MOSFET. Fig. 16 presents the result of the short-circuit test of the LCL switch with the inductor in series. The maximum di/dt is 0.75A/µs, and the peak current value is 10.9A. As can be observed, the current now has a limited growth rate, and the surge current value is much lower than that was measured in the test without the inductor. Nevertheless, the surge current is almost twice the limiting value.

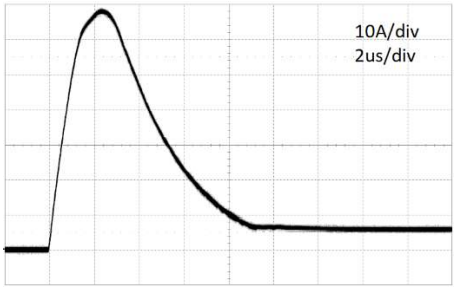

Fig. 15. Surge current applying reduced gate voltage (4.5V)

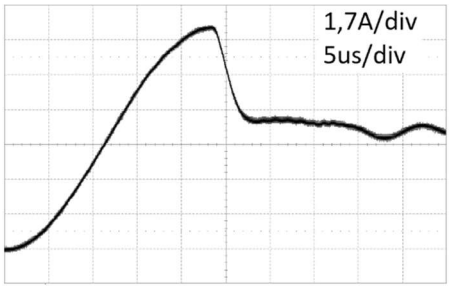

Fig. 16. Surge current using series inductor

The use of an inductor at the source terminal of the power MOSFET was the next step. The value of the inductor L_S is calculated using (3). It is notable that in this method, the supply voltage value does not influence the choice of the inductor. Considering the gate voltage of 6.2V and V_T of 3V (average between the values provided in the IRF5M4905 transistor manual [6]), the value of L_S should be 3.2µH. For convenience, a value of 2.2µH was used.

Fig. 17 presents the result of the short-circuit test of the LCL switch with the inductor at the source of the MOSFET. The maximum current slope is 0.8A/µs, and the peak current is 11.3A. The performance of the circuit is very similar to the case of using the series inductor, but tue value of the inductance is more than 10 times smaller.

To define the value of inductor L_S, the voltage limiting circuit on the source inductor (4) is used. In this type of circuit, the inductance value only depends on the parameters of the diode and the bipolar transistor. For the inductance calculation, it is assumed that the sum of the forward voltage drops across the diode (D_1) and the transistor (Q_1) is 1V. This assumption is valid since the circuit will bias the base of the transistor which, at low currents, has a high gain, on the order of 100 times or more. The value of L_S should be 1µH. Due to the unavailability of an inductor with a value close to the calculated one, the value of 2.2µH was used again. Fig. 18 shows the result of the short-circuit test of the LCL switch with voltage-limiting inductor at the source of the MOSFET. The maximum rate of current change is 0.26A/µs, and the peak current value is 8.8A.

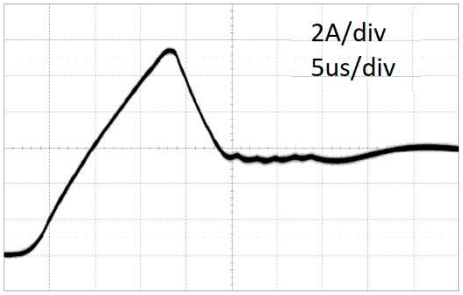

Fig. 17. Surge current using source inductor

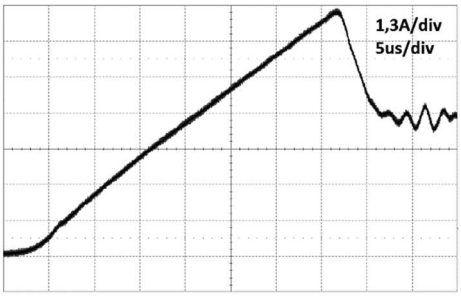

Fig. 18. Surge current using voltage limiting circuit on the source inductor

Among the three methods used to limit the di/dt, the use of an inductor at the source terminal of the power MOSFET appeared to be the most suitable to be associated with the predictive control. It has the smallest size among the candidate solutions and a lower number of components compared to the voltage-limiting inductor method. After the insertion of the 2.2µH inductor in series with the source terminal, the behavior of the switch showed significant improvement, as the circuit began to limit the di/dt. So, the predictive control was employed in association with the source inductor.

Fig. 19 shows the behavior of the switch during a short circuit after the insertion of the predictive control. As can be

observed, the predictive (or derivative) component in the control loop eliminated the current surge. The di/dt presented a maximum value of 0.8A/µs. Fig. 20 shows the final performance of the implemented LCL in a permanent short-circuit test. As can be observed, the LCL switch limits the short-circuit current, eliminates potential surges, and turns off the load after 2ms of the fault occurrence.

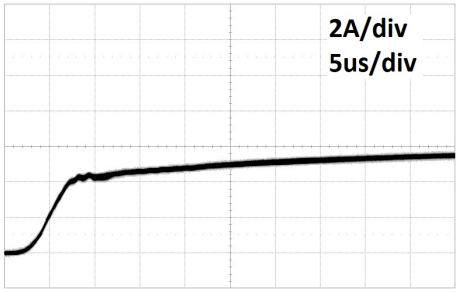

Fig. 19. Transient using source inductor and predictive control

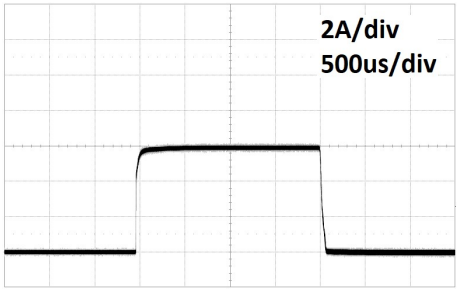

Fig. 20. Final performance of the implemented LCL switch

Table 1 presents a comparison between the results obtained from the applied methods. The reduction in V_{GS} was unable to control the di/dt or reduce the surge to an acceptable level. On the other hand, the three methods that employed inductors proved to be efficient in limiting current growth during a short circuit.

The use of an inductor in series with the switch is the most straightforward method and is not reliant on semiconductor parameters, making it more temperature-stable. However, the current growth limitation is dependent on the DC bus voltage, which can fluctuate. Furthermore, the inductance value is relatively high, resulting in a component with large physical dimensions, leading to increased mass and volume.

Using an inductor at the source terminal of the power MOSFET demonstrates performance comparable to that of the series inductor, with the added benefit of having a significantly lower value (more than an order of magnitude lower). This leads to a more compact circuit design. Moreover, this method is not affected by the DC bus voltage but is directly influenced by temperature, as it can affect the MOSFET parameters.

The method of implementing voltage limiting at the source inductor provides the most effective di/dt control, even when using a low inductance value. This approach is unaffected by DC bus voltage fluctuations. However, it is susceptible to temperature effects. Furthermore, it demands the use of a bigger number of active components, which contributes to an increase in circuit size and a potential decrease in reliability.

TABLE 1 – Comparison between the methods

	di/dt (A/us)	Peak (A)	Increasing in circuit	Surge
Reduced V_{GS}	50	68	-	high
Output inductor	0.75	10.9	high	low
Source inductor	0.8	11.3	low	low
Voltage limiting	0.26	8.8	high	low
Predictive control	0.8	-	low	-

IV. Conclusion

This work presented the design and validation process of an LCL switch, with a focus on controlling di/dt and eliminating the initial current surge. Although the circuit was used in a 28V DC bus, the considerations made here are also applicable to the development of protection switches for other types of DC power distribution systems.

The three methods presented for limiting the di/dt have proven to be functional. However, the method using the source inductor appears to be the most suitable solution due to the low inductance value, the reduced number of components, and the practical performance. Combining this solution with the appropriate choice of VGS voltage significantly attenuated the initial current surge while controlling the di/dt. This contributes to minimizing interference generation during a potential overload.

The addition of predictive control to the LCL switch's control loop significantly improved the circuit's response and eliminated the initial current surge. The proposed topology, using the source inductor and the predictive control for the LCL switch proved to be efficient, resulting in a circuit that met the desired requirements.

Acknowledgment

Participation in this event is financed by the São Paulo Research Foundation (FAPESP) grant 2021/11258-5 and by the National Council for Scientific and Technological Development (CNPq) grant nº 303859/2020-2.

References

[1] Ahmed T. Elsayed, Ahmed A. Mohamed, Osama A. Mohammed, DC microgrids and distribution systems: An overview, Electric Power Systems Research, Volume 119, 2015, Pages 407-417, ISSN 0378-7796, doi: 10.1016/j.epsr.2014.10.017.

[2] A. V. Dias, J. A. Pomilio and S. Finco, "A current limiting switch for applications in space power systems," 2017 IEEE Southern Power Electronics Conference (SPEC), Puerto Varas, Chile, 2017, pp. 1-6, doi: 10.1109/SPEC.2017.8333594.

[3] A. V. Dias et al., "Radiation Hardened Latching Current Limiter for Space Applications," 2023 IEEE Aerospace Conference, Big Sky, MT, USA, 2023, pp. 1-9, doi: 10.1109/AERO55745.2023.10115918.

[4] A. S. Sedra, K. C. Smith, Microelectronic Circuits, fifth edition, Oxford University Press, New York, 2004.

[5] M. Komatsu, N. Ide and S. Yanabu, "A Solid-State Current Limiting Switch for Application of Large-scale Space Power Systems," 2007 IEEE Power Electronics Specialists Conference, Orlando, FL, USA, 2007, pp. 1471-1476, doi: 10.1109/PESC.2007.4342211.

[6] IRF5M4905 - 55V, P-CHANNEL HEXFET MOSFET TECHNOLOGY, International Rectifier, http://www.irf.com/product-info/datasheets/data/irf5m4905.pdf, accessed in 26/08/2023.

[7] A. Elbanhawy, "Effect of Source Inductance on MOSFET Rise and Fall Times", Application demonstration, Maplesoft.

[8] A. V. Dias, " Chave de proteção com limitação de corrente para aplicações em sistemas espaciais," Ph.D. dissertation, FEEC, UNICAMP, Campinas, Brazil, 2012. [Online]. Available: https://repositorio.unicamp.br/Busca/Download?codigoArquivo=466263